USN

NEW SCHEME

Third Semester B.E. Degree Examination, Dec. 06 / Jan. 07
EC / EE / IT / BM / ML / CS / IS
Logic Design

Time: 3 hrs.] [Max. Marks:100

Note : *Answer any FIVE full questions.*

1 a. Prove the following :
   i) $\bar{a}c + \bar{a}b + \bar{a}c + ab = a\bar{b}$
   ii) $(a + b)(\bar{a}c + c)(\bar{b} + ac) = \bar{a}b$
   iii) $a\bar{b} + b\bar{c} + \bar{a}c = \bar{a}b + \bar{b}c + a\bar{c}$ (10 Marks)

   b. Implement
   i) $w = x\bar{y} + \bar{x}y$ using NAND gates
   ii) $w = (x + z)(\bar{y} + \bar{v})(\bar{w} + \bar{x} + \bar{y})$ using NAND (06 Marks)

   c. Simplify using Boolean algebra
   $\bar{w}\bar{x}yz + w\bar{x}\bar{y}z + xz + xy\bar{z}$ (04 Marks)

2 a. Identify all prime implicants and essential prime implicants of the following functions using K map.
   i) $f(a,b,c,d) = \Sigma m(0,1,2,5,6,7,8,9,10,13,14,15)$
   ii) $f(a,b,c,d) = \Pi m(0,2,5,8,9,10,12,14)$ (08 Marks)

   b. Find a minimal sum for the following Boolean function using Quine McCluskey method and prime-implicant table reduction
   $f(a,b,c,d) = \Sigma m(3,4,5,7,10,12,14,15) + \Phi(2)$ (12 Marks)

3 a. Find the minimal sum and minimal product using MEV technique using a,b,c as map variables
   $f(a,b,c,d) = \Sigma m(3,4,5,7,8,11,12,13,15)$ (08 Marks)

   b. Find minimal sum and minimal product for the following function using K-map
   $f(a,b,c,d) = \Sigma m(6,7,9,10,13) + dc(1,4,5,11,15)$ (08 Marks)

   c. Define :
   i) Positive logic
   ii) Negative logic (04 Marks)

4 a. With diagram, define
   i) Rise time
   ii) Fall time
   iii) Propagation delay
   iv) Fan-in
   v) Fan out. (10 Marks)

   b. Using NMOS draw the circuit for
   i) Inverter
   ii) NOR gate
   iii) NAND gate (06 Marks)

   c. Draw the circuit diagram for
   i) 2-input CMOS NOR
   ii) 2-input CMOS NAND (04Marks)

Contd.... 2

5 a. Construct 16:1 multiplexer using 4 tol and 2 tol multiplexer. **(04Marks)**

b. Implement the following using 4×4 PROM

Input (a, b)		Output (f_0, f_1, f_2, f_3)			
0	0	0	0	1	1
0	1	0	1	0	0
1	0	0	1	0	0
1	1	1	1	0	0

(04 Marks)

c. Implement $f(a,b,c,d) = \Sigma m(0,1,5,6,7,9,10,15)$ using

i) 8:1 MUX with a,b,c as select lines

ii) 4:1 MUX with a,b as select lines **(06 Marks)**

d. Design a 4 bit parallel fast look a head carry generator. **(06 Marks)**

6 a. Design a synchronous counter using JK flip flops to count in the sequence
0, 1, 2, 4, 5, 6, 0, 1, 2 . . . .
use state diagram and state table. **(08 Marks)**

b. Explain TTL with

i) Wired logic

ii) Open collector

iii) Totem pole output **(12 Marks)**

7 a. Give the logic diagram of

i) SR latch

ii) Gated D latch

iii) Master Slave JK flip flop

iv) Master Slave SR flip flop **(08 Marks)**

b. With diagram explain universal shift register. **(08 Marks)**

c. Explain the working of switch debouncer using SR latch. **(04 Marks)**

8 Write short notes on :

a. Ripple counter

b. PLA

c. Ring counter

d. Decoder. **(20 Marks)**